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Tips for Achieving Simulation Convergence With EPC Space Modular Products

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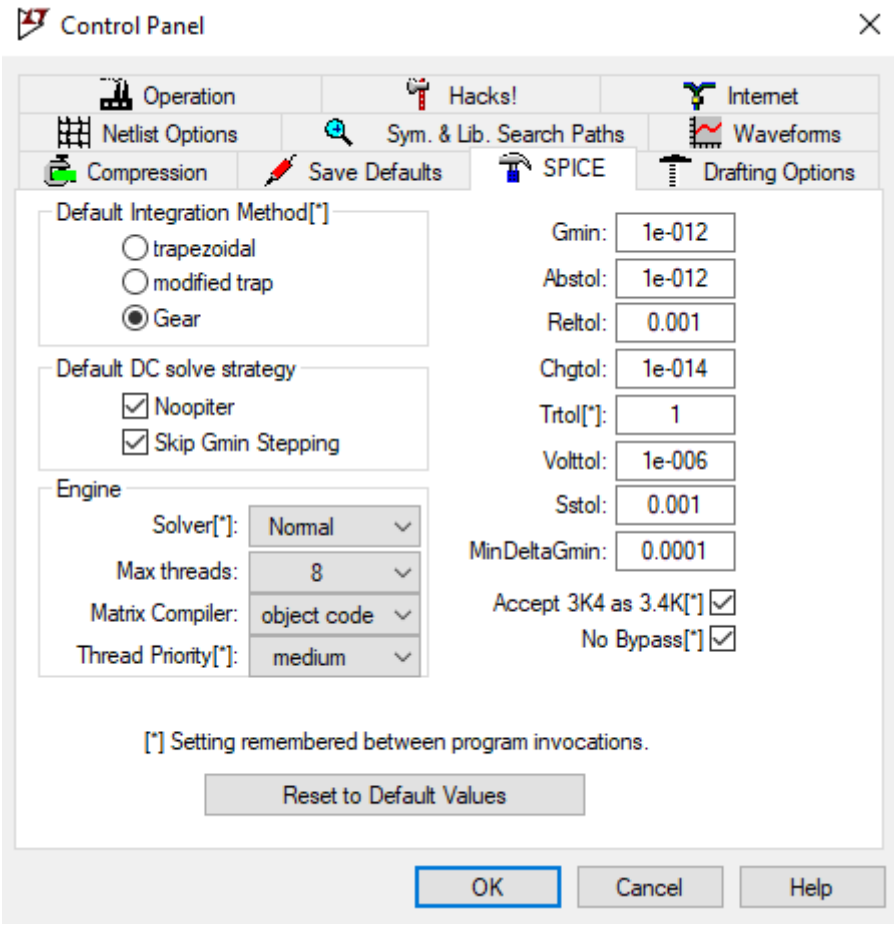
LT Spice Set-Up

- Prior to running an LT Spice simulation of a circuit containing an EPC Space module model, it is suggested to do the following:
- Set the “Default Integration Method[*]” to “Gear” by choosing that radio selection option.
- Set parameters “Noopiter” and “Skip Gmin Stepping” by checking their selection boxes:
  - From the LT Spice menu select Simulate, then Control Panel, the SPICE. (Simulate > Control Panel > SPICE);
  - In the “Default DC solve strategy” box in the SPICE tab, tick both the “Noopiter” and “Skip Gmin Stepping” boxes.
- Click “OK”.

LT Spice Set-Up



Simulation Power Supply Set-Up

- It is STRONGLY recommended that all bias sources (VBIAS and VDD) powering the EPC Space module models be provided with a finite ramp rate to the final value:
  - A linear or exponential ramp.
  - Suggest 1 us, minimum.
- This finite ramp rate serves to prevent convergence issues/problems at a sharp power supply application (i.e. t=0).
- All power supplies have some turn on “feature” with time:
  - They do not rise with infinite slew rate as may be (nearly) set with LT Spice model representations.
- Try to approximate and use the power supply slew rate(s) anticipated in the circuit.

Simulation Power Supply Set-Up

- In some cases just providing a finite power supply ramp rate is not sufficient to achieve consistent simulation convergence.
- If this situation is encountered, it is recommended to add a small resistance in series with the VDD power supply to aid with convergence.
  - 0.0005 Ohms is a good starting point
  - This resistance can be raised and lowered by trial-and-error to achieve the desired convergence stability.
- The requisite series resistance may be added with a discrete resistor or by adding parasitic series resistance in the “Independent Voltage Source” parametric box for the VDD power supply.

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